CLAIMS

1. An integrated circuit comprising:

a plurality of functional modules;

a bus for interconnecting said plurality of functional modules; and

a common buffer disposed on said bus for storing transfer information transferred between any functional modules within said plurality of functional modules.

2. An integrated circuit according to claim 1, wherein said common buffer is set in a buffering enabled state or a buffering disabled state depending on whether or not a buffer in a destination module can accept said transfer information.

3. An integrated circuit according to claim 2, further comprising means for selecting a path for transferring information to said destination module when a signal from said destination module indicates that the buffer within said destination module can accept information, and selecting a transfer path for storing said transfer information in said common buffer when the signal indicates that the buffer within said destination module cannot accept information.

4. An integrated circuit according to claim 1, further comprising a signal line for transferring said transfer information when a buffer within a destination module of said transfer information can accept a transfer, said signal line circumventing said common

buffer.

5. An integrated circuit according to claim 1, wherein said bus is arranged such that said common buffer within said bus is located adjacent to each of said plurality of functional modules within said integrated circuit.

6. An integrated circuit according to claim 1, further comprising means, operative when an information receiving buffer in a destination module cannot accept a transfer, for communicating information from said destination module to a source module, said information indicating that no transfer can be permitted.

7. An integrated circuit comprising, on a bus for transmitting transfer information between a plurality of functional modules:

a controlling unit for selecting a transfer path depending on whether or not a buffer in a destination module of said transfer data can accept said transfer information;

a common buffer for storing said transfer information transferred between said plurality of functional modules in accordance with the result of a selection made by said controlling unit; and

transfer path controlling means including a plurality of common bus interfaces for controlling input/output between said plurality of functional modules and said common buffer.

8. An information processing apparatus

comprising:

a plurality of functional modules;

a bus for interconnecting said plurality of functional modules; and

a common buffer for temporarily storing information transferred between any functional modules within said plurality of functional modules.

9. An integrated circuit comprising:

a plurality of functional modules; and

at least two on-chip buses for interconnecting said plurality of functional modules,

wherein a first bus and a second bus are interconnected through a bus adapter; and

functional modules connected to said first bus includes a CPU module, an external memory interface module, and said bus adapter.

10. An integrated circuit according to claim 9, wherein:

said first bus employs a protocol identical to a protocol employed by said second bus.

11. An integrated circuit according to claim 10, wherein:

an operating frequency of said first bus is an integer multiple of an operating frequency of said second bus.